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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,792	10/18/2001	Guillaume Royer	S1022/8246	9624

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EXAMINER	
LE, UYEN CHAU N	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,792	ROYER, GUILLAUME	
	Examiner	Art Unit	
	Uyen-Chau N. Le	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Requesting Continued Examination (RCE)

1. Receipt is acknowledged of the Requesting Continued Examination (RCE) field 25 April 2005.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-7, 16-18 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacson et al (US 5,708,419) in view of Hornstein et al (US 5,905,429).

Re claims 1-3, 6-7, 16-18 and 21-23: Isaacson et al discloses a self-adhesive electronic circuit including a planar base 26 having first and second base surfaces, an antenna 22 attached on the first surface of the base 26, a chip 14 connected to the antenna 22, a double faced adhesive 94 having first and second adhesive surfaces, wherein the first adhesive surface is glued on one of the base surfaces and the second adhesive surface forms an outward adhesive surface of the self-adhesive electronic circuit (i.e., the surface which is adhered to housing 92) (fig. 8; col. 9, line 58 through col. 10, line 25); wherein the chip 14 is glued on the first surface of the base and is

connected to the antenna by connection wires 44, the wires 44 and the chip 14 being covered with a drop of resin 45 (col. 9, lines 20-33); wherein an etched surface of the chip 14 faces the first surface of the base, and the chip 14 is connected to the antenna by welding beads/pads [38, 40, 42]; wherein the base 26 is made of a flexible sheet (col. 5, lines 25+); wherein the surface of the base 26 which does not receive the double faced adhesive is provided to receive printing of a pattern (e.g., cover label 96), of a text or of a code (fig. 8; col. 10, lines 4+); the double-faced adhesive 94 having an opening/cutout, wherein at least a portion of the antenna 22 is disposed in the opening/cutout (fig. 8); the electronic chip 14 disposed at least partially in the opening/cutout and electrically coupled to the antenna 22; wherein the electronic chip is spaced from and does not contact the double faced adhesive (see fig. 8); wherein the double faced adhesive comprises a double faced adhesive tape (col. 10, lines 15+).

Isaacson et al is silent with respect to a protective cover, which is removable to expose the second adhesive surface as an outward adhesive surface of the self-adhesive electronic circuit.

Hornstein et al teaches a label comprises a double-sided adhesive layer 40, a chip 25, a coil 224 and a protective layer 41, which is removable to expose the second adhesive surface as an outward adhesive surface of the label so that the label can be affixed to a product (figs. 1 & 9-10; col. 6, lines 41-63 and col. 7, line 33 through col. 8, line 10).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate a protective cover, which is removable to expose the second adhesive surface as an outward adhesive surface of the label of Hornstein et al

into the system as taught by Isaacson et al in order to provide Isaacson et al with a more secure system wherein the tag/label can be affixed and secured to a product via the adhesive surface, thus preventing the tag/label from being separated from the product during handling and/or transporting, and therefore an obvious expedient.

4. Claims 4-5 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacson et al as modified by Hornstein et al as applied to claims 1 and 16 above, and further in view of Launay (US 6,111,303). The teachings of Isaacson et al as modified by Hornstein et al have been discussed above.

Re claims 4-5 and 19-20: Isaacson et al/Hornstein et al have been discussed above but fails to teach or fairly suggest that the chip is placed in a slot made through the base, the chip is connected to the antenna by welding beads located in connection slots going through the base.

Launay teaches a chip 9 being placed within a cavity/slot made through a base 1 having a surface 2; the chip 9 connecting to an antenna 4 via connection slots through the base 1 (fig. 1; col. 3, line 22+).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the teachings of Launay into the an electronic circuit as taught by Isaacson et al/Hornstein et al in order to provide Isaacson et al/Hornstein et al with a more compact system wherein the thickness of the card being reduced due to part of the thickness of the chip is disposed within the base via the cavity/hole.

1. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacson et al as modified by Hornstein et al as applied to claim 1 above, and further in view of

Vieilledent (US 4,701,236). The teachings of Isaacson et al as modified by Hornstein et al have been discussed above.

Re claim 8, Isaacson et al/Hornstein et al have been discussed above but fails to teach or fairly suggest a method of manufacturing the self-adhesive electronic circuit, wherein the attachment of the double faced adhesive on the base includes the steps of: forming a rectangle of double faced adhesive including an opening, gluing the adhesive rectangle on a packaging protective film, ungluing the adhesive rectangle from the protective film, and assembling the adhesive on the base.

Vieilledent teaches a rectangular double-faced adhesive 1 provided with two protective layers 2, 3 including an opening 4; the protective layer 3 is moved and the tape 1 is glued to a base/film 5, then an IC chip 6 is mounted in a cavity 11 of the base/film 5 (figs. 2A-2D; col. 3, lines 10+).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the teachings of Vieilledent into the teachings of Isaacson et al/Hornstein et al because such modification would have been an obvious engineering variation, well within the ordinary skill in the art, for better handling a double-faced adhesive tape during manufacturing process (i.e., protective layers/films prevent the tape from being glued to an undesired component and can be removed/peel-off readily without damaging the adhesive tape), and therefore an obvious expedient.

2. Claims 9-11 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacson et al as modified by Hornstein et al as applied to claim 1

above, and further in view of Murohara (US 6,089,461). The teachings of Isaacson et al as modified by Hornstein et al have been discussed above.

Re claims 9-11 and 14-15: Isaacson et al/Hornstein et al has been discussed above but fails to teach or fairly suggest that the thickness of the double faced adhesive is greater than or equal to the height of the electronic chip or the resin.

Murohara teaches a portion of an antenna 2 is disposed in the opening, which is filled with resin agent 4 and the thickness of adhesive agent 14 is greater than the height of the electronic chip 3 or the resin 4 (figs. 4-6; col. 4, lines 17-63).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the teachings of Murohara into the teachings of Isaacson et al/Hornstein et al in order to improve the strength against bending and enhance the protection capability of the chip and/or antenna in the event the card is bended.

3. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacson et al as modified by Hornstein et al and Murohara as applied to claim 9 above, and further in view of Launay (US 6,111,303). The teachings of Isaacson et al as modified by Hornstein et al and Murohara have been discussed above.

Re claims 12-13: Isaacson et al/Hornstein et al/Murohara have been discussed above but fails to teach or fairly suggest that the chip is placed in a slot made through the base, the chip is connected to the antenna by welding beads located in connection slots going through the base.

Launay teaches a chip 9 being placed within a cavity/slot made through a base 1 having a surface 2; the chip 9 connecting to an antenna 4 via connection slots through the base 1 (fig. 1; col. 3, line 22+).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the teachings of Launay into the an electronic circuit as taught by Isaacson et al/Hornstein et al/Murohara in order to provide Isaacson et al/Hornstein et al/Murohara with a more compact system wherein the thickness of the card being reduced due to part of the thickness of the chip is disposed within the base via the cavity/hole.

4. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaacson et al as modified by Hornstein et al as applied to claim 16 above, and further in view of Appalucci et al (US 5,142,270). The teachings of Isaacson et al as modified by Hornstein et al have been discussed above.

Re claim 24: Isaacson et al/Hornstein et al have been discussed above and further disclose that the outward adhesive surface of the self-adhesive electronic circuit is adhered to the undersurface of the housing 92 (fig. 8; col. 9, lines 66-67), but is silent with respect to the undersurface of the housing is a non-planar surface.

Appalucci et al teaches a resonant tag circuit 10 comprises a base 12 having a first surface 16 and a second surface 18, a conductor 20 is attached to the first surface 16 of the base 12; an adhesive layer 34 having a first surface and a second surface, the first surface of the adhesive layer 34 is adhered to the surface 16 of the base 12, the second surface of the adhesive layer 34 forms an "outward" adhesive surface of the tag 10 and is covered with a removable liner 32; the liner 32 is removed prior adhering the

"outward" adhesive surface of the tag 10 to a surface of an article, wherein the surface of the article can be a non-planar surface (figs. 1 & 2; col. 4, lines 21-41 and col. 5, lines 53-60).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the teachings of Appalucci et al into the system as taught by Isaacson et al/Hornstein et al in order to provide Isaacson et al with a reliable system which can be utilized on a non-planar surface. Furthermore, such modification would provide Isaacson et al/Hornstein et al with the ability for securing the tag to a non-planar surface, thus providing confidence to users in traveling (i.e., the users do not have to concern about loosing their luggage due to the luggage's tag falls off), and therefore an obvious expedient.

Response to Arguments

5. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Newly cited references to Hornstein et al have been used in the new ground rejection to further meet the newly added limitation of the claimed invention (i.e., claims 1, 10 and 19-31).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The patents to Uenaka et al (US 5299940 A); Lee-Own et al (US 5500375 A); Hagiiiri-Teiirani et al (US 5514240 A); and Clapper (US 6693515 B2) are as of interest and illustrate to a similar structure of an apparatus and system of a self-adhesive electronic circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uyen-Chau N. Le whose telephone number is 571-272-2397. The examiner can normally be reached on Mon-Fri. 5:30AM-2:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Uyen-Chau N. Le
June 12, 2005